Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1. (currently amended) A method comprising:

receiving a serial stream of data bits;

deserializing the serial stream of data bits into parallel bits;

inputting the parallel bits into a content addressable memory and a first register during a single clock cycle;

inputting an output of the first register into a second register;

inputting outputs of the first and second registers to the content addressable memory, wherein the parallel bits, output of the first register, and output of the second register are combined and stored as a first parallel word in a first row of the content addressable memory;

providing a bus configured to receive the parallel bits and output of the first register, wherein the data lines forming the bus are grouped into a plurality of overlapping subsets of the bus that each contain at least one common data line;

providing the parallel bits and the output of the first register in a plurality of parallel bit outputs onto the bus;

providing a set of parallel words stored in the content addressable memory, wherein at least one of the set of parallel words includes a fixed frame alignment detection pattern having a data position;

simultaneously comparing the first parallel word to the set of parallel words stored in the content addressable memory to detect a frame alignment pattern in the first parallel word; and

when the frame alignment pattern is detected in the first parallel word, selecting one of the subsets and associated parallel bit outputs based on match flag outputs from the content addressable memory, wherein each of the match flag outputs are associated with a

respective one of the set of parallel words that includes the matching frame alignment pattern and the matching data position with respect to the frame alignment pattern of the first parallel word.

2. (previously presented) The method of claim 1 wherein the plurality of parallel bits and the output of the first register are input to a plurality of tristate driver circuits, and wherein selecting one of the subsets and the associated parallel bit outputs comprises:

enabling one of the tristate driver circuits to output the parallel bits and the output of the first register associated with that tristate driver circuit to an output bus, and disabling other ones of the tristate driver circuits coupled to the output bus.

3. (original) The method of claim 1 wherein there are eight parallel bits.

4. (original) The method of claim 1 wherein the first and second registers are two stages of a shift register.

5. (original) The method of claim 1 wherein a depth of the content addressable memory comprises at least one row for each of the parallel bits.

6. (original) The method of claim 1 wherein the inputs to the content addressable memory are provided by way of parallel transfer.

7. (original) The method of claim 6 wherein a width of the parallel bits inputting the content addressable memory is at least a number of parallel bits output from the deserializer plus a length of a pattern to be detected using the content addressable memory minus 1.

8. (currently amended) A circuit comprising:

a deserializer circuit coupled to receive serial data input and outputting a first parallel data output, wherein the deserializer circuit outputs the first parallel data onto a bus that is configured with overlapping subsets of the bus, wherein the subsets include at least one common data line;

a shift register coupled to the first parallel data output; and

a content addressable memory~~,~~ that is coupled to an output of the shift register and that receives ~~to receive~~ the first parallel data output in parallel with the parallel output of the shift register, wherein the parallel output of the shift register is stored as part of a first parallel word in a first row of the content addressable memory that is simultaneously compared to a set of parallel words employed by the content addressable memory to detect a pattern within the first parallel word, wherein each parallel word of the set of parallel words includes a fixed data pattern to detect the pattern in the first parallel word, wherein each fixed data pattern includes a respective data position within a respective data word.

9. (previously presented) The circuit of claim 8 further comprising:

a plurality of second parallel data outputs based on the first parallel data output, wherein each of second parallel data outputs are associated with a respective one of the subsets; and

a plurality of tristate buffer circuits, one coupled to each of the subsets of the bus.

10. (original) The circuit of claim 9 further comprising:

a control logic block, coupled to a match signal from the content addressable memory, generating a plurality of select signals, one coupled to each of the tristate buffer circuits.

11. (original) The circuit of claim 10 wherein based on the match signal, the control logic block generates select signals to enable one of the tristate buffers and disable others of the tristate buffers.

12. (original) The circuit of claim 10 wherein the control logic block comprises a state machine.

13. (previously presented) The circuit of claim 9 wherein there is one parallel data output for each bit of the first parallel data output minus 1.

14. (original) The circuit of claim 8 wherein the shift register is divided into three portions, the first portion of the shift register is coupled to the deserializer, the second portion of the shift register is coupled to the first portion through a first multiplexer, and the third portion of the shift register is coupled to the second portion through a second multiplexer.

15. (previously presented) The circuit of claim 14 wherein the third portion of the shift register is coupled to the first portion of the shift register through the second multiplexer.

16. (previously presented) The circuit of claim 14 wherein the second portion of the shift register is coupled to the deserializer through the first multiplexer.

17. (original) The circuit of claim 8 wherein each row in the content addressable memory comprises a data pattern to be detected in the serial data input.

18. (original) The circuit of claim 8 wherein the content addressable memory has a number of rows equal to or greater than a number of bits of the first parallel data output.

19. (original) The circuit of claim 8 wherein the content addressable memory comprises a bit pattern comprising "1111," "0110," "0010," and "1000" in at least a number of rows that is equal to a number of bits of the first parallel data output.

20. (original) The circuit of claim 8 wherein the first parallel data output is 8, 10, 16, or 20 bits wide.

21. (original) A programmable logic integrated circuit comprising the circuit of claim 8.

22. (original) The circuit of claim 8 further comprising:

a plurality of parallel data output formats based on the first parallel data output; and

a selector circuit, coupled to each of the parallel data output formats and the first parallel data output, outputting one of the parallel data output formats as a second parallel data output based on an output from the content addressable memory.

23. (original) The circuit of claim 8 wherein the first parallel data output comprises 8 bits in a format bit 0, bit 1, bit 2, bit 3, bit 4, bit 5, bit 6, and bit 7, and the circuit further comprises:

a first parallel data output format comprising bit 1, bit 2, bit 3, bit 4, bit 5, bit 6, bit 7, and bit 0;

a second parallel data output format comprising bit 2, bit 3, bit 4, bit 5, bit 6, bit 7, bit 0, and bit 1; and

a third parallel data output format comprising bit 3, bit 4, bit 5, bit 6, bit 7, bit 0, bit 1 and bit 2;

a fourth parallel data output format comprising bit 4, bit 5, bit 6, bit 7, bit 0, bit 1, bit 2, and bit 3;

a fifth parallel data output format comprising bit 5, bit 6, bit 7, bit 0, bit 1, bit 2, bit 3, and bit 4;

a sixth parallel data output format comprising bit 6, bit 7, bit 0, bit 1, bit 2, bit 3, bit 4, and bit 5; and

a seventh parallel data output format comprising bit 7, bit 0, bit 1, bit 2, bit 3, bit 4, bit 5, and bit 6.

24. (currently amended) A method comprising:

deserializing an input serial data stream into a first parallel word;

storing the first parallel word in a register;

deserializing the input serial data stream into a second parallel word;

~~generating a second parallel word from the first parallel word;~~

grouping the first parallel word and the second parallel word into a plurality of data word subsets that overlap to include at least one common data bit;

generating a third parallel word from the combination of the first parallel word and the second parallel word, wherein the third parallel word is wider than the first parallel word and the second parallel word;

storing the third parallel word in a first row of a content addressable memory;

detecting a frame alignment symbol within the third parallel word by simultaneously comparing the third parallel word to a plurality of fixed frame alignment patterns, wherein each of the fixed frame alignment patterns are part of a respective one of a set of parallel words stored in a the content addressable memory.

25. (previously presented) The method of claim 24, further comprising selecting one of the subsets associated with a respective one of the frame alignment patterns that matches the frame alignment symbol.

26. (previously presented) The method of claim 24, wherein detecting the frame alignment symbol comprises detecting the frame alignment symbol within one clock cycle.

27. (previously presented) The method of claim 24, wherein grouping the second parallel word comprises outputting the second parallel word on a data bus that includes subsets of data lines that correspond to the data word subsets.